

Read head and evaluation unit VAA-2E-IER2-S-1M-V1

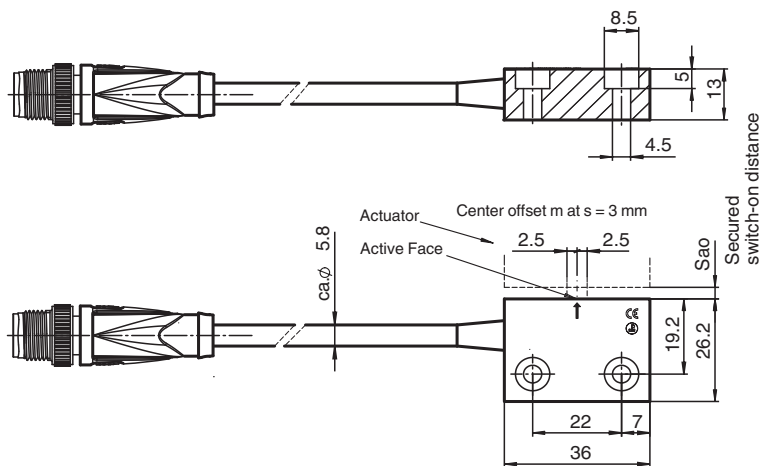


- Small plastic housing
- Encapsulated electronics
- Especially suited to small doors and coverings
- Multiple-flush magnet system
- Cable with M12 plug

Reed safety switch for non-contact AS-Interface safety switches



Dimensions



Technical Data

General specifications

Detection type		magnetic
assured start-up distance	S _{a0}	7 mm
assured release distance	S _{ar}	max. 40 mm
Center offset	m	± 2.5 mm at distance s = 3 mm
Node type		Safety node
AS-Interface specification		V3.0
Required gateway specification		≥ V2.0
Profile		S-0.B
IO code		0
ID code		B
ID1 code		F
ID2 code		E
Response delay		< 5 ms
UL File Number		E155795
Functional safety related parameters		
Safety Integrity Level (SIL)		SIL 3

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Refer to "General Notes Relating to Pepperl+Fuchs Product Information".

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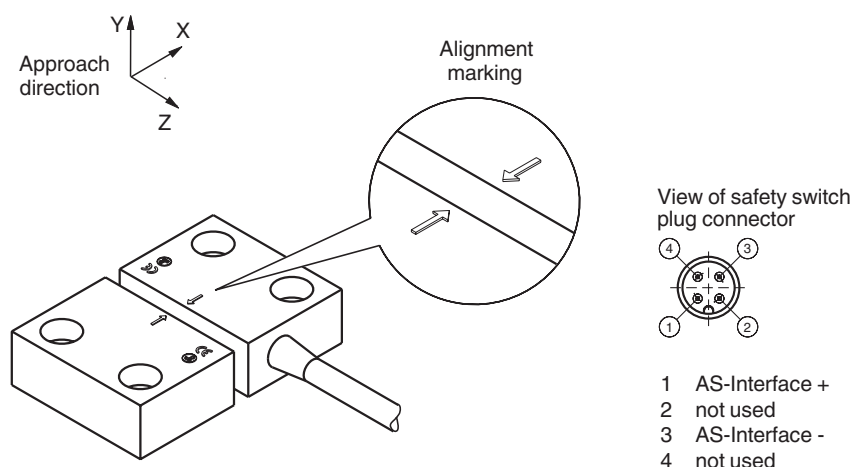
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Technical Data

Performance level (PL)		PL e
Mission Time (T _M)		20 a
PFH _d		4.29 E-8
Electrical specifications		
Rated operating voltage	U _e	26.5 ... 31.6 V from AS-Interface
Rated operating current	I _e	≤ 30 mA
Power supply		via AS-Interface network
Directive conformity		
Electromagnetic compatibility		
Directive 2014/30/EU		EN 62026-2:2013+A1:2019 EN 60947-5-3:2013
Machinery Directive		
Directive 2006/42/EC		EN ISO 13849-1:2015 EN ISO 14119:2013
Standard conformity		
Degree of protection		EN 60529:2000
AS-Interface		EN 62026-2:2013+A1:2019
Functional safety		ISO 13849-1:2008 (up to category 3/PL e) EN ISO 12100-1, -2:2003 EN 1088:1995+A2:2008
Ambient conditions		
Ambient temperature		-20 ... 60 °C (-4 ... 140 °F)
Shock and impact resistance		30 g/11 ms
Mechanical specifications		
Degree of protection		IP67
Connection		with fixed cable and M12 connector, 4-pin
Material		
Housing		PPS
Cable		PUR
Installation		any position
Dimensions		
Width		26.2 mm
Depth		13 mm
Length		36 mm
Cable length		1 m
Life span		100 x 10 ⁶ switching cycles

Assembly





Data bit	Input
D0	dyn. safety code 1
D1	dyn. safety code 1
D2	dyn. safety code 2
D3	dyn. safety code 2

Parameter bit	Function
P0	IN1
P1	IN2
P2	IN3
P3	IN4